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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,405	04/14/2000	Eiji IO	APM-01301	8514

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EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/550,405

Applicant(s)

IO, EIJI

Examiner

ori nadav

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 20-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 20-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-11 and 20-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support for all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6, because the specification does not recite any first or second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate and has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-11 and 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of said at least one first/second drain and source region, as recited in claims 1 and 6, are unclear as to whether applicant refers to the at least one lightly/heavily doped second drain and source region, or to other regions.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-6, 9-11, 20 and 22, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez (5,439,835) in view of Cheng et al. (5,545,575).

Regarding claims 1, 3, 5, 6, 9 and 11, Gonzalez teaches in figure 9 and related text a memory cell semiconductor device comprising:

- (a) a semiconductor substrate 12;
- (b) an insulating film 13 formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode 16 formed on said semiconductor substrate, said gate electrode and said insulating film can define at least one lightly doped first drain and source diffusion layer;

(d) at least one sidewall covering said gate electrode therewith; and

(e) at least one heavily doped second drain and source diffusion layer formed at a surface of said semiconductor substrate around said gate electrode,

said at least one sidewall 41 (see figure 4) having connected thereto a sidewall offset extending outwardly of said gate electrode along the surface of said semiconductor substrate in at least one of regions below which said at least one second drain and source diffusion layer is to be formed, said sidewall offset having a lateral dimension extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a thickness of said sidewall,

(f) low resistive wiring layers 92, 51 (figure 5) formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset,

said at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate,

wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

Gonzalez does not teach at least one lightly doped first drain and source diffusion layer contacts said at least one second drain and source diffusion layer on at least a bottom and a lateral side, and at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset.

Cheng et al. teach in figure 7 at least one lightly doped first drain and source diffusion layer 43, 44 contacts said at least one second drain and source diffusion layer 57, 58 on at least a bottom and a lateral side, and at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form at least one lightly doped first drain and source diffusion layer contacts said at least one second drain and source diffusion layer on at least a bottom and a lateral side, as taught by Cheng et al., wherein at least one lightly doped first drain and source diffusion layer extending towards said gate electrode beyond an edge of said sidewall offset, in Gonzalez's device, in order to improve the device characteristics by forming LDD regions in the device, and in order adjust and optimize the device characteristics by extending the first drain and source diffusion layers towards the gate electrode beyond an edge of the sidewall offset.

Regarding claims 4 and 10, Cheng et al. teach in figure 7 second diffusion layers 43, 44 of lower impurity concentration than that of the source and drain regions 57, 58 (column 4, lines 24-26 and column 6, lines 2-4) formed below the source and drain regions.

Regarding claim 6, Cheng et al. teach in figure 7 silicide wiring layers 64 formed at surfaces and in the source and drain layers located outwardly beyond a peripheral edge of the sidewall offset. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form silicide wiring layers at surfaces and in the source and drain layers located outwardly beyond a peripheral edge of the sidewall offset in Gonzalez's device in order to reduce the contact resistance of the device.

Regarding claims 20 and 22 Gonzalez teaches in figure 9 only one sidewall offset.

3. Claim 7, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez and Cheng et al., as applied to claim 6 above, and further in view of Kunishima et al. (5,316,977).

Gonzalez and Cheng et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Gonzalez and Cheng et al.'s device,

because titanium silicide is a conventional silicide material, of which official notice is taken.

4. Claims 1-4, 6, 8-10, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. Cheng et al. teach in figure 15 a semiconductor device comprising:

- (a) a semiconductor substrate 11;
- (b) an insulating film 19 formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;
- (c) a gate electrode 28 formed on said semiconductor substrate, said gate electrode and said insulating film defining at least one lightly doped first drain and source diffusion layer 77', 78';
- (d) at least one sidewall 66 covering said gate electrode therewith; and
- (e) at least one heavily doped second drain and source diffusion layer 82, 84 formed at a surface of said semiconductor substrate around said gate electrode, said at least one sidewall having connected thereto a sidewall offset extending outwardly of said gate electrode along the surface of said semiconductor substrate in at least one of regions below which said at least one second drain and source diffusion layer is to be formed, said sidewall offset having a lateral dimension extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a thickness of said sidewall,



(f) low resistive wiring layers 64 formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset,

said at least one heavily doped second drain and source diffusion layer extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate,

wherein all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

Cheng et al. do not teach in the embodiment of figure 15 first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and a lateral side and extending towards the gate electrode beyond an edge of the sidewall offset.

Cheng et al. teach in the embodiment of figure 7 first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom and a lateral side, wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, in Cheng et al.'s device, in order to improve the

device characteristics by forming LDD regions in the device, and in order adjust and optimize the device characteristics by extending the first drain and source diffusion layers towards the gate electrode beyond an edge of the sidewall offset.

Regarding claims 21 and 23, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

5. Claims 5, 7, 11, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al., as applied to claims 1 and 6 above, and further in view of Kunishima et al.

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice may be taken.

Regarding claims 5 and 11, Kunishima et al. teach using the semiconductor device as a CMOS device, and it is well known in the art that CMOS devices are used as memory devices. It would have been obvious to a person of ordinary skill in the art at the time

the invention was made to use Cheng et al.'s device as a memory device, because the intended use of a device depends on the requirements of the application in hand.

Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 21 and 23, Kunishima et al. teach in figure 5C a sidewall entirely covering the gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

### ***Response to Arguments***

Applicant argues that prior art does not teach that all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6.

. There is no support for the claimed limitations of all of said at least one second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6, because the specification does not recite any first or second drain and source diffusion layer that is exposed to said surface of said semiconductor substrate and has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.  
July 13, 2004

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PATENT EXAMINER  
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